# Modeling, Design and Implementation of a Twoport DC-DC Converter with Synchronized PWM Control

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Abstract— This paper presents modeling, design and implementation of a two-port DC-DC converter with synchronized PWM voltage mode analog control. The proposed PWM control strategy provides simultaneous dual regulated output voltages for boost and buck modes of operation from a single input. The dynamics of the two-port DC-DC converter is modeled with small signal analysis. A type-II and type-III analog compensators are designed for the boost mode and for the buck mode operations of the converter respectively. The proposed control strategy is experimentally validated in an experimental setup for a boost output of 60V and buck output of 15V with an input voltage of 30V for an output power of 150W. The closed loop performance of the converter is demonstrated for a load change of 2A and input voltage variation of ±5V i.e., ±15% of line voltage variation.

**Index Terms**— Two-port DC-DC converter, buck–boost converter, control-to-output transfer function, PI controller, Analog Compensator, Synchronized PWM, small signal analysis

# 1 INTRODUCTION

Multi-port DC-DC converters have gained a significant importance in renewable energy sector [1-2]. Nowadays, most of the consumer products require power supplies at different level of voltages/ currents for different user specific loads [3]. The multi-port converter topologies are classified mainly in two categories non-isolated and isolated topologies. The non- isolated multiport converter topologies use buck, boost and buckboost topologies.

To obtain different output voltages, the concept of replacing the main switch of a buck converter by a halfbridge network is reported in [4]. The two-port DC-DC converter topology [5] which investigates the architectural advantages by replacing the main switch of a boost converter with a half-bridge network and generates two outputs, step-up as well as step-down from a single DC input. Isolated bi-directional multi-port converters are constructed out of full bridge network for relatively high power applications [7-10]. However, full bridge based topologies require more number of switching devices and increase control complexity. The isolated multi-port converters using bridge topologies have the advantages of high efficiency with ZVS [9]. However, most of the works reported are on open loop operation and lack on synchronized control strategy among different converter stages. An open loop converter cannot regulate its output voltage for the variation in input voltage and change in load. A detailed approach utilizing state space averaging method to obtain converter model is presented in [11]. The positive feedback effect due to the RHP zero and the methods to minimize its effects are described in [12]. Selection of compensation network type and its synthesis are explained in [13].

Authors in [14] study the operation of multi-port DC-DC converter by using single type compensator. However, it is observed experimentally that step-up output of the converter is not stable with a type-3 compensator due to the presence of right half plane (RHP) zero. Therefore, it is important to develop decoupled model for each stage of multi-port converter and design suitable synchronized controller for each stage to control each output independently. Dynamic behaviors of multi-port power

electronic interface under line and load disturbances are discussed in [15].

This paper presents a decoupled model, design and synchronized voltage mode control of a non-isolated two-port DC-DC converter. The decoupled model of the two-port DC-DC converter is developed based on small signal analysis. A type-2 compensator for boost part and a type-3 compensator for buck part of the converter are chosen and designed respectively. The proposed synchronized PWM control strategy achieves fast dynamic response and stable outputs from each stage of the converter. The triangular carrier wave used in [14] is replaced with a saw-tooth carrier wave which generates synchronized PWM control signals for the switches and makes the charging and discharging cycle of inductor smoother. The schematic of the non-isolated two-port DC-DC converter topology [14] used is shown in Fig.1.

Section 2 and 3 provide a brief description on the modes of operation, steady state analysis and the small signal modeling of the converter with selection of analog compensators respectively. A new synchronized PWM voltage mode analog control is proposed and explained in section 4. Section 5 presents design implementation and result analysis of the proposed synchronized PWM control strategy with a two-port converter in open and closed loop configuration under steady state and transients. Section 6 concludes the paper.

# 2. PRINCIPLE OF OPERATION OF TWO-PORT DC-DC CONVERTER

#### A. Modes of Operation

The two port DC-DC converter has two series connected power semiconductor switches  $(Q_1, Q_2)$  as shown in Fig.1. Hence it results in four possible operating states based upon the status of these switches, either turned on or turned off. Out of these four states, three are distinct states and thus results in three distinct modes of operation.

- Mode I –both Q1 and Q2 are ON
- Mode II –Q1 is ON and Q2 is OFF
- Mode III –both Q1 and Q2 are OFF

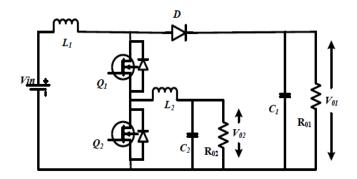


Fig.1 Two-Port DC-DC Converter

The duration for which the switch  $Q_1$  is ON is defined by the duty ratio (D<sub>1</sub>+D<sub>2</sub>) and the duration for which switch  $Q_2$  is ON is defined by the duty ratio D<sub>1</sub>. The typical waveforms of the switch node voltages, the inductor and the diode currents, and the voltage across the inductor, during the different modes of operation of the converter are illustrated in Fig. 2.

#### B. Steady State Analysis

For the purpose of steady state analysis, the small ripple approximation for the inductor currents and capacitor voltages are assumed to be zero. Thus, the gain expressions for the two outputs can be derived from the inductor volt second balance equations, as shown below. For inductor L<sub>1</sub>, from Fig. 2, it can be inferred that, during Mode-I, the voltage across L<sub>1</sub> is  $v_{in}$  and during the rest of the time, it is  $(v_{in}-v_{01})$ .

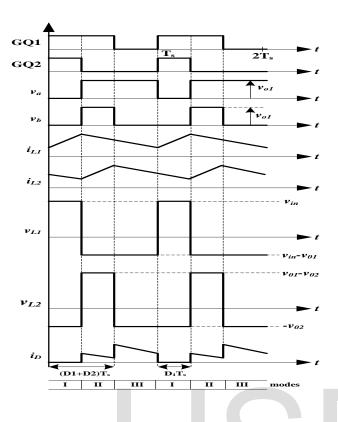


Fig. 2 Waveforms of the switch node voltages, the inductor current and voltage and the diode currents.

Thus,

$$(v_{in} \times D_1) + (v_{in} - v_{o1}) \times (1 - D_2) = 0$$

$$\frac{v_{o1}}{v_{in}} = \frac{1}{(1-D_1)} \tag{1}$$

Similarly, for inductor L2, from Fig. 2, it can be inferred that, during Mode-II, the voltage across L2 is  $(v_{o1} - v_{o2})$  and during the rest of the time it is $(-v_{o2})$ . Thus,

$$(v_{o1} - v_{o2}) \times D_2 + (-v_{o2}) \times (1 - D_2) = 0$$
$$\frac{v_{o2}}{v_{o1}} = D_2$$
(2)

Therefore,

$$\frac{v_{o2}}{v_{in}} = \frac{v_{o2}}{v_{o1}} \times \frac{v_{o1}}{v_{in}} = \frac{D_2}{(1 - D_1)}$$
(3)

From (1) and (3), it can be inferred that the two DC outputs obtained from the converter are boost and buck output respectively. The boost output depends upon the interval when both switches are turned "ON" simultaneously (dependent upon duty D<sub>1</sub>), whereas the buck output is regulated solely using switch Q1, when Q2 is "OFF" (dependent upon both D<sub>1</sub> and D<sub>2</sub>). For any particular value of the duty cycle D<sub>1</sub>, the step-down conversion ratio varies within the range:

$$0 \le \frac{V_{o2}}{V_{in}} \le 1 \tag{4}$$

The buck output of the converter depends on both the duty ratios  $D_1$  and  $D_2$  instead of a single duty ratio as in a conventional buck converter. Thus, the output voltage has a wider range i.e., from 0 to1 at the acceptable duty ratios of the switch.

Similarly, the step-up conversion ratio varies between:

$$1 \le \frac{V_{o1}}{V_{in}} \le \frac{1}{(1 - D_1)} \tag{5}$$

The sum of duty cycles should satisfy the following condition as they share the same switching period.

$$D_1 + D_2 \le 1 \tag{6}$$

To study the dynamics of the two-port DC-DC converter, modeling of the converter is presented in next section.

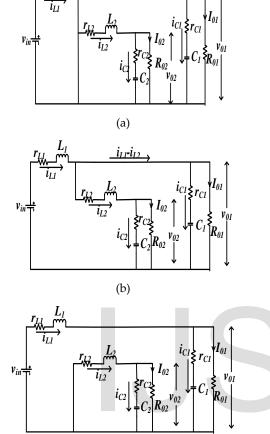
# 3. Modeling of Two-Port DC-DC Converter

There are various methods to model a switch mode DC-DC converter into linear time invariant systems. State space averaging, Circuit averaging, Current injected approach is some of them. In this work state space averaging technique is considered for modeling the two port DC-DC converter. The details of state space modeling are described in next.

#### A. State space modeling

The converter has three distinct operational modes and thus three equivalent circuits are analyzed for the modeling of the converter. The currents through the inductors  $i_{L1}$  and  $i_{L2}$  and the voltage across the capacitor  $v_{C1}$  and  $v_{C2}$  are considered as the state variables. The equivalent circuit diagram during the first, second and

third modes of operation are given in Fig. 3(a), 3(b) and 3(c) respectively.



(c)

Fig. 3 Equivalent circuit of the twoi-port dc-dc converter at different modes. The figure shows the equivalent circuit during (a) Mode I of duration  $D_1T_{s_r}$  (b) Mode II of duration  $D_2T_s$  and (c) Mode III of duration  $(1-D_1-D_2)T_s$ .

#### 1) Structure I:

The circuit during the first mode of operation is as given in Fig. 3(a). The state space equations for this structure is derived as follows

$$\frac{di_{L1}}{dt} = -\frac{r_{L1}}{L_1}i_{L1} + \frac{v_{in}}{L_1}$$
(7)
$$\frac{di_{L2}}{dt} = -i_{L1}\left[\frac{r_{L2}(R_{02} + r_{C2}) + r_{C2}R_{02}}{L_2(R_{02} + r_{C2})}\right] - v_{C2}\frac{R_{02}}{(R_{02} + r_{C2})}$$

$$\frac{dv_{C1}}{dv_{C1}} = v_{C1} + v_{C1} + v_{C2} + v_{C2$$

$$\frac{dv_{C1}}{dt} = -\frac{v_{C1}}{C_1(R_{01} + r_{C1})}$$
(9)  
$$\frac{dv_{C2}}{dt} = i_{L1}\frac{R_{02}}{C_2(R_{02} + r_{C2})} - \frac{v_{C2}}{C_2(R_{02} + r_{C2})}$$
(10)

$$\begin{bmatrix} di_{L1} \end{bmatrix}$$

The above equations can be written as,

$$\begin{bmatrix} \overline{dt} \\ \underline{di}_{L2} \\ \overline{dt} \\ \overline{dv}_{C1} \\ \overline{dt} \\ \overline{dv}_{C2} \\ \overline{dt} \end{bmatrix} = \begin{bmatrix} -r_{L1} & 0 & 0 & 0 \\ 0 & -\left[ \frac{r_{L2}(R_{02} + r_{C2}) + r_{C2}R_{02}}{L_2(R_{02} + r_{C2})} \right] & 0 & -\frac{R_{02}}{L_2(R_{02} + r_{C2})} \\ 0 & 0 & -\frac{1}{C_1(R_{01} + r_{C1})} & 0 \\ 0 & \frac{R_{02}}{C_2(R_{02} + r_{C2})} & 0 & \frac{-1}{C_1(R_{01} + r_{C1})} & \frac{-1}{C_2(R_{02} + r_{C2})} \end{bmatrix} \\ + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_{in}] \\ \begin{bmatrix} v_{01} \\ v_{02} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{R_{01}}{R_{01} + r_{C1}} & 0 \\ 0 & \frac{r_{C2}R_{02}}{R_{02} + r_{C2}} & 0 & \frac{R_{02}}{R_{02} + r_{C2}} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix}$$

Above equations can be rewritten as,

$$\dot{x} = A_1 x + B_1 u$$
 (11)  
 $\dot{y} = C_1 x + D_1 u$  (12)

#### 2) Structure II:

The circuit during the second mode of operation is as given in Fig. 3(b). The state space equations for this structure is derived as follows

$$\frac{di_{L1}}{dt} = \frac{v_{in}}{L_1} - \frac{i_{L1}}{L_1} \left[ r_{L1} + \frac{r_{C1}R_{01}}{R_{01} + r_{C1}} \right] + \frac{i_{L2}}{L_1} \left[ \frac{r_{C1}R_{01}}{R_{01} + r_{C1}} \right] - \frac{v_{C1}}{L_1} \left[ \frac{R_{01}}{R_{01} + r_{C1}} \right]$$
(13)

$$\frac{di_{L2}}{dt} = \frac{i_{L1}}{L_2} \left[ \frac{r_{C1}R_{01}}{R_{01} + r_{C1}} \right] - \frac{i_{L2}}{L_2} \left[ r_{L2} + \frac{r_{C2}R_{02}}{R_{02} + r_{C2}} + \frac{r_{C1}R_{01}}{R_{01} + r_{C1}} \right] \\ + \frac{v_{C1}}{L_2} \left[ \frac{R_{01}}{R_{01} + r_{C1}} \right] \\ - \frac{v_{C2}}{L_2} \left[ \frac{R_{02}}{R_{02} + r_{C2}} \right]$$
(14)

$$\frac{dv_{C1}}{dt} = \frac{i_{L1}}{C_1} \left[ \frac{R_{01}}{R_{01} + r_{C1}} \right] - \frac{i_{L2}}{C_1} \left[ \frac{R_{01}}{R_{01} + r_{C1}} \right] - \frac{v_{C1}}{C_1} \left[ \frac{1}{R_{01} + r_{C1}} \right]$$
(15)

$$\frac{dv_{C2}}{dt} = i_{L1} \frac{R_{02}}{C_2(R_{02} + r_{C2})} - \frac{v_{C2}}{C_2(R_{02} + r_{C2})}$$
(16)

The above equations can be written as,

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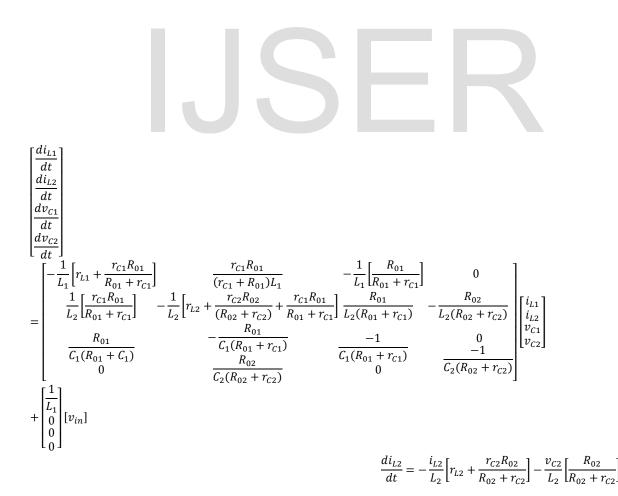
$$\dot{x} = A_2 x + B_2 u \tag{17}$$

$$\dot{y} = C_2 x + D_2 u \tag{18}$$

#### *3) Structure III:*

The circuit during the third mode of operation is as given in Fig. 3(c). The state space equations for this structure are derived as follows.

$$\frac{di_{L1}}{dt} = \frac{v_{in}}{L_1} - \frac{i_{L1}}{L_1} \left[ r_{L1} + \frac{r_{C1}R_{01}}{R_{01} + r_{C1}} \right] - \frac{v_{C1}}{L_1} \left[ \frac{R_{01}}{R_{01} + r_{C1}} \right]$$
(19)



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$$\frac{dv_{C1}}{dt} = \frac{i_{L1}}{C_1} \left[ \frac{R_{01}}{R_{01} + r_{C1}} \right] - \frac{v_{C1}}{C_1} \left[ \frac{1}{R_{01} + r_{C1}} \right]$$
(21)

$$\frac{dv_{C2}}{dt} = i_{L1} \frac{R_{02}}{C_2(R_{02} + r_{C2})} - \frac{v_{C2}}{C_2(R_{02} + r_{C2})}$$
(22)

The above equations can be written as,

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{c1}}{dt} \\ \frac{dv_{c2}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{L_1} \begin{bmatrix} r_{L1} + \frac{r_{c1}R_{01}}{R_{01} + r_{c1}} \end{bmatrix} & 0 \\ = \begin{bmatrix} -\frac{1}{L_1} \begin{bmatrix} r_{L1} + \frac{r_{c1}R_{01}}{R_{01} + r_{c1}} \end{bmatrix} & 0 \\ \frac{R_{01}}{C_1(R_{01} + C_1)} & \frac{R_{02}}{C_2(R_{02} + r_{c2})} \end{bmatrix} & 0 \\ = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} r_{p1}(1 - D_1) & -r_{p2}D_2 & \frac{r_{p1}}{r_{c1}} & 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} r_{p2} & 0 & \frac{r_{p2}}{r_{c2}} \end{bmatrix} \\ 0 & -\frac{1}{L_1} \begin{bmatrix} \frac{R_{01}}{R_{01} + r_{c1}} \end{bmatrix} & 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} \frac{1}{L_1} \begin{bmatrix} r_{L1} + \frac{r_{c2}R_{01}}{R_{01} + r_{c1}} \end{bmatrix} \\ 0 \\ \frac{R_{01}}{C_1(R_{01} + C_1)} & \frac{R_{02}}{C_2(R_{02} + r_{c2})} \end{bmatrix} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} \frac{1}{L_1} \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} r_{p1}(1 - D_1) & -r_{p2}D_2 & \frac{r_{p1}}{r_{c1}} & 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$\begin{bmatrix} v_{01} \\ v_{02} \end{bmatrix} = \begin{bmatrix} \frac{r_{C1}R_{01}}{R_{01} + r_{C1}} & 0 & \frac{R_{01}}{R_{01} + r_{C1}} & 0 \\ 0 & \frac{r_{C2}R_{02}}{R_{02} + r_{C2}} & 0 & \frac{R_{02}}{R_{02} + r_{C2}} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix}$$

Above equations can be rewritten as,

$$\dot{x} = A_3 x + B_3 u \tag{23}$$

 $\dot{y} = C_3 x + D_3 u \tag{24}$ 

The converter has three modes of operation and the duration of each mode is  $D_1T_s$ ,  $D_2T_s$  and  $(1-D_1-D_2)$  Ts respectively. Thus, the state space average model of the converter is given as,

$$\begin{aligned} \dot{x} &= Ax + Bu \\ \dot{y} &= Cx + Du \end{aligned} \tag{25}$$

where,

 $+ \begin{vmatrix} L_1 \\ 0 \\ 0 \end{vmatrix} [v_{in}]$ 

$$A = A_1 D_1 + A_2 D_2 + A_3 (1 - (D_1 + D_2))$$
(27)  

$$B = B_1 D_1 + B_2 D_2 + B_3 (1 - (D_1 + D_2))$$
(28)  

$$C = C_1 D_1 + C_2 D_2 + C_3 (1 - (D_1 + D_2))$$
(29)

Substituting the values of A1, A2, A3, B1, B2, B3, C1, C2 and C3 in (27), (28) and (29), we get,

#### **B. Small Signal Modeling**

 $r_{L1} - r_{p1}(1 - D_1)$ 

 $L_1$ 

L<sub>2</sub>

 $r_{p_1}D_1$ 

 $r_{p1}(1-D_1)$ 

 $r_{c1}c_{1}$ 

 $L_1$ 

 $L_2$ 

 $r_{p_1}D_2$ 

 $\frac{r_{c1}c_1}{r_{p2}}$ 

 $-r_{p_1}D_2-r_{L2}$ 

The equations derived above are non-linear and we have to linearize them. To linearize and obtain small signal model we have to perturb them around a steady operating point. Let.

Let,	
$v_{in} = v_{in_0} + \Delta v_{in}$	(30)
$i_{01} = i_{01_0} + \Delta i_{01}$	(31)
$i_{02} = i_{02_0} + \Delta i_{02}$	(32)
$d_1 = d_{1_0} + \Delta d_1$	(33)
$d_2 = d_{2_0} + \Delta d_2$	(34)
Therefore,	
$x = x_0 + \Delta x$	(35)
$u = u_0 + \Delta u$	(36)
$A = A_0 + \Delta A$	(37)
$B = B_0 + \Delta B$	(38)

Substituting, (35), (36), (37) and (38) in the state equation,  $\dot{x_0} + \Delta \dot{x} = (A_0 + \Delta A)(x_0 + \Delta x) + (B_0 + \Delta B)(u_0 + \Delta u)$   $0 + \Delta \dot{x} = A_0 x_0 + B_0 u_0 + A_0 \Delta x + \Delta A x_0 + B_0 \Delta u + \Delta B u_0$  $+ \Delta A \Delta x + \Delta B \Delta u$ 

 $\Delta A \Delta x + \Delta B \Delta u$  is expected to be zero under steady state. For small signal model we consider only first order terms and thus we obtain

$$\Delta \dot{x} = A_0 \Delta x + \Delta A x_0 + B_0 \Delta u + \Delta B u_0 \tag{39}$$

By substituting, the corresponding values in the above equation and simplifying it, we get,

0

 $r_{p2}$ 

 $L_2 r_{c2}$ 

0

 $r_{p_1}(1-D_1)$ 

 $r_{c1}L_1$ 

 $r_{p_1}D_2$ 

 $r_{c1}L_2$ 

 $-r_{p_{1}}$ 

$$\begin{bmatrix} \Delta i_{L1} \\ \Delta i_{L2} \\ \Delta v_{C1} \\ \Delta v_{C2} \end{bmatrix} = [A] \cdot \begin{bmatrix} \Delta i_{L1} \\ \Delta i_{L2} \\ \Delta v_{C1} \\ \Delta v_{C2} \end{bmatrix} + [B_1] \cdot \Delta d_1 + [B_2] \cdot \Delta d_2$$
$$+ \begin{bmatrix} 1 \\ L_1 \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_{in}]$$
(40)

$$\begin{bmatrix} \Delta v_{01} \\ \Delta v_{02} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \Delta i_{L1} \\ \Delta i_{L2} \\ \Delta v_{C1} \\ \Delta v_{C2} \end{bmatrix}$$
(41)

Step- Up Output	45V
Voltage(vo1)	
Step- Down Output	15V
Voltage(vo2)	
Step- Up DC Load(i01)	2A
Step- Down DC Load(io2)	2A
Switching Frequency	20kHz
Power	120W

where,

We have,

$$\begin{bmatrix} A \end{bmatrix} = \begin{bmatrix} r_{L1} - r_{p1}(1 - D_1) & r_{p1}D_2 & -r_{p2} - r_{p1}D_2 - r_{L2} & r_{p1}D_2 & -r_{p2} \\ \hline L_1 & & L_1 & & r_{p1}D_2 & -r_{p2} \\ \hline r_{p1}D_1 & & -r_{p2} - r_{p1}D_2 - r_{L2} & r_{p1}D_2 & -r_{p2} \\ \hline r_{p1}C_1 & & L_2 & & r_{p1}D_2 & -r_{p2} \\ \hline r_{p1}C_1 & & -r_{p1} & 0 \\ \hline r_{p1}C_1 & & & -r_{p1} & 0 \\ \hline r_{p1}C_1 & & & r_{p2} \\ \hline r_{p1}C_1 & & & r_{p1} \\ \hline r_{p1}C_1 & & & r_{p2} \\ \hline r_{p1}C_1 & & & r_{p2} \\ \hline r_{p1}C_1 & & & r_{p2} \\ \hline r_{p1}C_1 & & & r_{p1} \\ \hline r_{p1}C_1 & & & r_{p2} \\ \hline r_{p1}C_1 & & & r_{p2} \\ \hline r_{p2}C_2 \\ \hline r_{p1}C_1 & & & r_{p2} \\ \hline r_{p1}C_1 & & & r_{p2} \\ \hline r_{p2}C_2 \\ \hline r_{p1}C_1 & & & r_{p2} \\ \hline r_{p1}C_1 & & & r_{p1} \\ \hline r_{p1}C_1 & & & r_{p1} \\ \hline r_{p1}C_1 & & & r_{p2} \\ \hline r_{p1}C_1 & & & & r_{p2} \\ \hline r_{p2}C_2 \\ \hline r_{p2}C_2 \\ \hline r_{p1}C_1 & & & & r_{p2} \\ \hline r_{p1}C_1 & & & & \\ \hline r_{p1}C_1 & & & & \\ \hline r_{p1}C_1$$

$$[B_2] = \begin{bmatrix} \frac{i_{L1}r_{p1}}{L_1} \\ \frac{v_{01}r_{p1}}{L_1r_{c1}} + \frac{i_{L1}r_{p1}}{L_2} - \frac{i_{L2}r_{p1}}{L_2} \\ -\frac{i_{L2}r_{p1}}{r_{c1}C_1} \\ 0 \end{bmatrix}$$

 $[C_1] = [0 \quad 0 \quad 1 \quad 0] \quad ; \quad [C_2] = [0 \quad 0 \quad 0 \quad 1]$ 

#### C. Transfer Function Derivation of the two port DC-**DC converter**

The design specification of the two port DC-DC converter is as given in the TABLE I.

Input Voltage(vin)	30 V
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$$R_{o2} = \frac{V_{o2}}{I_{o2}}$$
(47)

$$=\frac{15}{2}=7.5\Omega$$

 $i_{L2} = I_{o2} = 2A$ 

 $R_{o1} = \frac{V_{o1}}{I_{o1}} = \frac{45}{2} = 22.5\Omega$ 

# 1) Designing of $L_1$

The voltage across the inductor  $L_1$  is given by the formula,

(45)

(46)

$$v_{L1} = L_1 \frac{di_{L1}}{dt}$$
(48)

$$\therefore \Delta i_{L1} = \frac{1}{L_1} \int v_{L1} dt \tag{49}$$

During the interval defined by the time duration  $D_1T_s$ , the voltage across the inductor is  $v_{in}$ . Therefore, the change in inductor current is given as,

$$\Delta i_{L1} = \frac{1}{L_1} V_{in} D_1 T_s \tag{50}$$

$$\Delta i_{L1} = \frac{V_{in}D_1}{f_s L_1} \tag{51}$$

Thus, the value of inductor *L*<sup>1</sup> is derived as,

$$\therefore L_1 = \frac{V_{in}D_1}{\Delta i_{L1}f_s} \tag{52}$$

Substituting the design parameters and considering allowable inductor current ripple, we get  $L_1$ =1.2mH.

2) Designing of  $L_2$ 

The voltage across the inductor  $L_2$  is given by the formula,

$$v_{L2} = L_2 \frac{di_{L2}}{dt} \tag{53}$$

During the interval defined by the time duration  $D_2T_s$ , the voltage across the inductor is given as,

$$v_{L2} = v_b - V_{o2}$$
(54)  

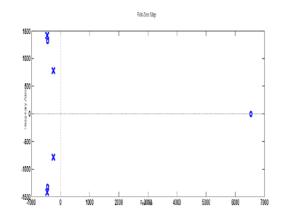
$$v_{L2} = V_{o1} - V_{o2}$$
(55)

Therefore, the change in inductor current is given as,

$$\Delta i_{L2} = \frac{1}{L_2} (V_{o1} - V_{o2}) \frac{D_2 T_s}{2}$$
$$\Delta i_{L2} = \frac{(V_{o1} - V_{o2})D_2}{2L_2 f_s}$$
(56)

Thus, the value of inductor *L*<sup>2</sup> is derived as,

$$\therefore L_2 = \frac{(V_{o1} - V_{o2})D_2}{2\Delta i_{L2} f_s}$$
(57)



Substituting the design parameters and considering allowable inductor current ripple, we get  $L_2$ =1.125mH.

The small signal model of the converter by substituting the parameters to it, the control-to-output transfer function of the boost and buck outputs are obtained as given below,

$$\begin{split} & \frac{\Delta v_{01}(s)}{\Delta d_1(s)} \\ &= \frac{-4226s^3 + 4.852e7s^2 + 3.096e10s + 9.397e13}{s^4 + 1276s^3 + 3.244e6s^2 + 1.527e9s + 1.463e12} \\ & \frac{\Delta v_{02}(s)}{\Delta d_2(s)} \\ &= \frac{2.274e - 12s^3 + 8.33e7s^2 + 3.551e10s + 6.358e13}{s^4 + 1276s^3 + 3.244e6s^2 + 1.527e9s + 1.463e12} \end{split}$$

#### D. Compensator for boost part of the converter

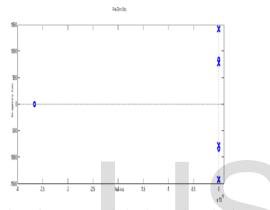
The boost converter offers a new set of complications in analysis and characteristics and can be a challenging converter to stabilize when operating with voltage-mode control. Right-half-plane (RHP) zero has additional constraints on the design of loop compensation and crossover frequency. With an RHP zero in the control-to-output transfer function, the control loop does not respond immediately to any change. The bandwidth of the loop must be limited to considerably less than the frequency of the RHP zero if the system is to be stabilized properly. Pole-zero and Bode-plot of the control-to-output transfer function for boost part of the system is shown in Fig.4(a) and 4(b) respectively.

# (a)

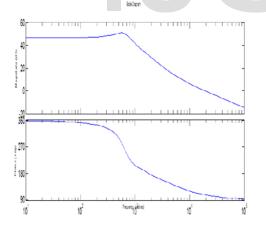
(b)

Fig.4 (a) Pole –zero plot (b) Bode-plot of boost part of the converter

It is observed that the phase boost required at the cross over frequency is 64<sup>o</sup> which is less than 90<sup>o</sup>. Therefore, a type-II compensator as shown in Fig. 5 is chosen for boost part of the converter. The cross-over frequency is fixed at 4 kHz which is one-fifth of the



switching frequency and also lesser than the frequency at which the right-half-plane (RHP) zero exists.



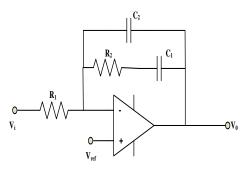
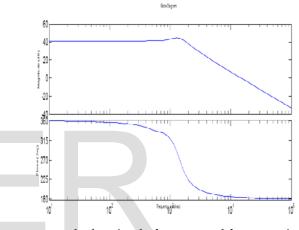


Fig. 5 A Type II Compensator

# E. Compensator for buck part of the converter

Pole-zero and Bode-plot of the control-



to-output transfer function for boost part of the system is shown in Fig.6(a) and 6(b) respectively. The required phase boost is determined from the Bode-plot of the control-to-output transfer function of buck part of the system as well. It is observed that the phase boost required at the cross over frequency is 105° which is greater than 90° and less than 180°. Therefore, a type-III compensator as shown in Fig. 7 is designed for the buck part of the converter with the cross-over frequency at 4 kHz which is one-fifth of the switching frequency.

(a)

(b)

Fig. 6 (a) Pole-Zero (b) Bode- plot for the buck part of the converter

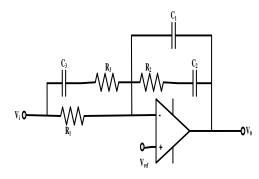


Fig.7 A type III compensator

#### F. Comparison of Analog Compensators with Digital Compensators

Digital compensators are limited to about 10 kHz unity gain frequency. It can get really fast with ADC/DAC cards but processing and integration becomes a challenging issue. It also has limitations with the dynamic range which is limited even for a best system to about 20-bits. Furthermore, it often needs good whitening both at ADC and DAC. Whereas, analog systems are robust. It has good dynamic range and also processing is continuous as there is no inherent bandwidth limit.

Considering the above mentioned cons of digital control and the pros of analog control, we have considered an analog voltage mode synchronized PWM control for the two-port DC-DC converter.

# 4. PROPOSED SYNCHRONIZED PWM CONTROL

Closed loop control is a process of making a system variable to operate at a particular desired value using negative feedback. This involves measuring the system variable, obtaining the error signal and then influencing the value of the system variable using the error signal. The control-to-output transfer functions of the boost and the buck output of the converter derived above, are similar to those of the conventional boost and buck converter respectively. Thus, a synchronized PWM control scheme which directly uses the control scheme of conventional buck and boost converter is proposed. In this two modulating signals ( $v_{GQ1_mod}$  and  $v_{GQ2_mod}$ ) are compared with the same carrier waveform, in order to produce two synchronized triggering pulses as shown in Fig. 8 such that, switch  $Q_1$  is provided with a PWM

signal of duty  $(D_1 + D_2)$  and  $Q_2$  is provided with a signal of duty  $D_1$ .

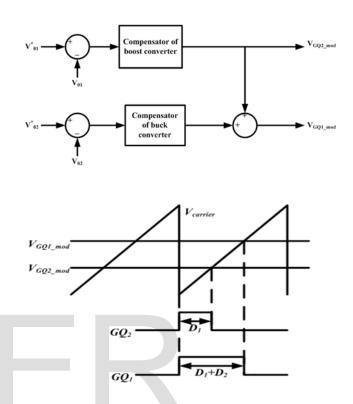


Fig. 8 Synchronized PWM Control Strategy

Two modulating signals are generated from two independent analog compensators. The task of the analog compensator is to shape the loop gain such that it has a crossover frequency at the desired place with enough phase and gain margins for a good dynamic response, line and load regulation and stability. The phase shift and the gain provided by each of these compensators vary and they are suitably selected based on the pole zero location of the converter for which the feedback loop has to be implemented. In this work two separate analog compensators are selected and designed for controlling the two outputs of the converter simultaneously.

Closed loop operation of two-port DC-DC converter with synchronized voltage mode control using analog compensators is presented in next section.

# 5. HARDWARE PROTOTYPE AND RESULTS

A 120W, 20 kHz, integrated dual output converter with input 30V and boost output of 45V and buck output of 15V, along with the analog compensator circuit is designed and implemented to validate the reliability of the compensators. The schematic of the complete circuitry is as shown in the fig. 9. Independent functionality of the integrated dual output of the converter is verified for constant duty ratio  $D_1$ = 0.66 while varying duty ratio  $D_2$ .

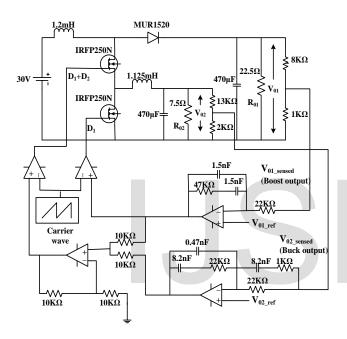


Fig. 9 Complete schematic of the Prtototype Design

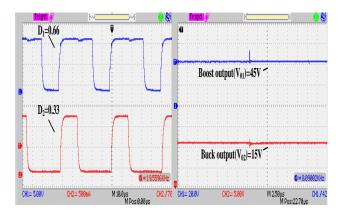


Fig. 10 Output voltages for an input of 30V and duty ratios  $D_1$ =0.66 and  $D_2$ =0.33

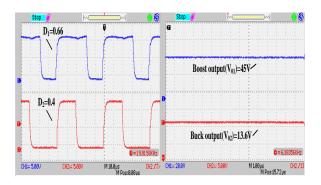


Fig. 11 Output voltages for an input of 30V and duty ratios  $D_1=0.66$  and  $D_2=0.4$ 

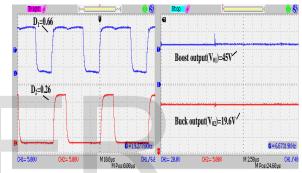


Fig. 12 Output voltages for an input of 30V and duty ratios  $D_1+D_2=0.66$  and  $D_1=0.26$ 

The performance of the analog compensators during steady state and transient operation of the converter in closed loop are tested with varying input voltage and load. The Fig.13 illustrates the variation in duty ratio (D1) with the change in input voltage. The transient operation of the integrated dual output converter in closed loop is demonstrated by step change in input voltage and load in Fig. 14 and Fig. 15. It is observed that the output voltages of the converter are regulated at steady state value. The line regulation of the system is verified by a step change in the input voltage. The compensators vary the duty ratios D1 and D2 with the change in input voltage in order to reach the output voltages steady state. The load regulation is verified by a step change in one of the loads and maintaining the other constant. Here the boost output is subjected to a load change of 2A while maintaining the buck constant. From the output obtained, it is observed that the compensators are able to exhibit crossregulation of the outputs.

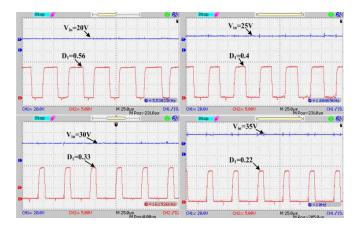


Fig. 13. Variation in duty ratio with variation in input voltage

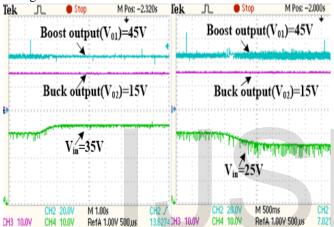


Fig. 14 Transient Response for change in input voltage

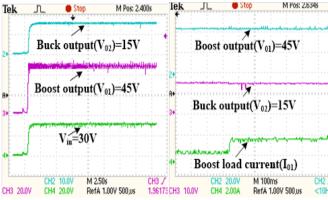


Fig. 15. Transient Response for a step input and load current

The variation of duty ratios ( $D_1$  and  $D_2$ ) with the variation in input voltage are depicted in Fig. 16. The overall efficiency of the converter obtained is 95%. The hardware prototype of the design is shown in Fig. 17.

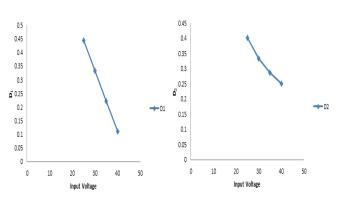
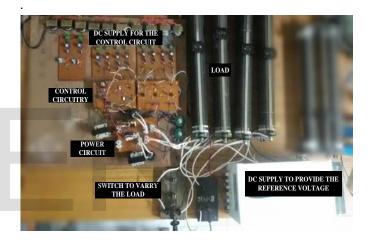


Fig. 16 Variation in duty ratio for the variation in input in order to maintain constant output voltages.





# 6. CONCLUSION

This work presents modeling, design and implementation of two-port DC-DC converter. Small signal analysis is performed to study the dynamics of the system and design of the compensators for the converter. A synchronized voltage mode PWM control is implemented using analog compensators for stable operation during transient. Open loop and closed loop operation of the converter are tested and demonstrated with hardware results.

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